ABSTRACT

Refresh of memory cells is performed periodically by a refresh timer, and collision between memory access and memory refresh is avoided. When memory access occurs, an F/F 163 is set by a one shot pulse from an OS circuit 161, a memory access request is inputted to a memory accessing pulse generator circuit 171 through a NOR gate 167, and a latch control signal LC and an enable signal REN are outputted. When a refresh request from the refresh timer is inputted to an AND gate 168 during the memory access, the output of the NOR gate 167 is at the "L" level, and the refresh request is blocked by the AND gate 168. Thereafter, at the time when the latch control signal LC is turned into the "L" level, F/Fs 163, 164 and 165 are reset, the output of the NOR gate 167 is turned into the "H" level, the refresh request is inputted to a refreshing pulse generator circuit 170, and a refresh enable signal RERF is outputted.